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ABSTRACTIMPROVED METHOD FOR TESTING FOR THE  
PRESENCE OF FAULTS IN DIGITAL CIRCUITS

A method of testing for the presence of faults in digital logic circuits is described. The method involves re-ordering a number of test vectors for testing digital circuits by selecting faults at random from an original fault list to form a sample fault list  $F_N$  and then forming a vector set  $T_{N-1}$  and then simulating the vector set  $T_{N-1}$  against the fault list  $F_N$ . Any vector from the set  $T_{N-1}$  which does not detect any fault is discarded and the remaining vectors are saved as vector set  $T_N$ . The method steps are repeated  $N$  times (with  $N$  having a value of 1 to  $M$ ). Duplicated vector patterns in each vector set are removed and then the final vector set is initialised to produce a final vector set  $T_f$ .

Embodiments of the invention are described.